

**REMARKS**

Claims 2-21 were pending in this application.

Claims 2-7, 12-17, 20, and 21 have been rejected.

Claims 8-11, 18, and 19 have been objected to.

Claims 5, 15, and 20 have been amended as shown above.

Claims 2-21 remain pending in this application.

Reconsideration and full allowance of Claims 2-21 are respectfully requested.

**I. INTERVIEW SUMMARY**

The Examiner and the Applicant's representative (the undersigned attorney) discussed this patent application on August 4, 2005. The Examiner indicated that this patent application was being withdrawn from appeal and that prosecution was being reopened. The Examiner indicated that a new non-final Office Action citing new art would be issued.

**II. ALLOWABLE CLAIMS**

The Applicant thanks the Examiner for the indication that Claims 8-11, 18, and 19 would be allowable if rewritten in independent form. Because the Applicant believes that the remaining claims in this application are allowable, the Applicant has not rewritten Claims 8-11, 18, and 19 in independent form.

### III. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 2-7 and 12-17 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,475,823 to Amerson et al. (“*Amerson*”). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP* § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP* § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)).

Claims 2 and 12 recite detecting an “instruction that loads data from a first memory location that was previously stored to,” where the instruction is detected “without requiring computation of an external memory address of said first memory location for the instruction.”

The Office Action asserts that the § 102 rejection of Claims 2-7 and 12-17 over *Amerson* is based on “the interpretation and a new argument that *Amerson* had implicit teaching of without calculation.” (*Office Action*, Page 8, Paragraph 21).

First, the Office Action contains inconsistent statements regarding the teachings of *Amerson*. The Office Action asserts that *Amerson* anticipates all elements of Claims 2 and 12. (*Office Action*, Pages 8-9, Paragraphs 21-22). The Office Action also states, more than once, that *Amerson* does not recite specific elements of Claims 2 and 12. (*Office Action*, Page 4, Section 8; Page 6, Section 16).

Second, the Office Action once again attempts to distinguish between “arithmetic” and “logic” operations performed in *Amerson*. The Office Action argues that *Amerson* detects load and store instructions that access the same memory location by comparing the actual memory addresses accessed by both instructions. The Office Action then makes the assertion that the comparison itself (or the flag representing a result of the comparison) does not require the computation of the actual memory addresses. Based on this, the Office Action asserts that *Amerson* anticipates detecting an “instruction that loads data from a first memory location that was previously stored to ... without requiring computation of an external memory address of said first memory location for the instruction” as recited in Claims 2 and 12.

Every single embodiment of *Amerson* compares the actual memory addresses being accessed by the load and store instructions. If the actual memory addresses being accessed are compared, those actual memory addresses must have been computed by some component in *Amerson*. In other words, it is impossible in *Amerson* to compare the actual memory addresses without first computing the actual memory addresses. It is also irrelevant which component of *Amerson* computes the actual memory addresses. The only issue that is relevant is whether an instruction that accesses a memory location can be detected in *Amerson* “without requiring computation of an external memory address” of that memory location as recited in Claims 2 and 12.

It is clear that the actual memory addresses being accessed in *Amerson* must be computed before those memory addresses can be compared. Because of this, detecting load and store instructions that access the same memory location in *Amerson* requires computation of the actual

memory addresses. As a result, the detection of the load and store instructions in *Amerson* cannot possibly occur “without requiring computation of an external memory address” as recited in Claims 2 and 12.

For these reasons, the Office Action fails to show that *Amerson* anticipates the Applicant’s invention as recited in Claims 2 and 12 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 2-7 and 12-17.

#### IV. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 2 and 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,854,921 to Pickett (“*Pickett*”) in view of *Amerson*. The Office Action rejects Claims 2-7 and 12-17 under 35 U.S.C. § 103(a) as being unpatentable over *Amerson* in view of *Pickett*. The Office Action rejects Claims 2-7 and 12-17 under 35 U.S.C. § 103(a) as being unpatentable over *Amerson* in view of U.S. Patent No. 5,706,224 to Srinivasan et al. (“*Srinivasan*”). The Office Action rejects Claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,850,138 to Engebretsen et al. (“*Engebretsen*”) in view of U.S. Patent No. 5,615,357 to Ball (“*Ball*”). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP* § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP*

§ 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (MPEP § 2142).

A. THE PICKETT-AMERSON AND AMERSON-PICKETT COMBINATIONS

As noted above in Section III, *Amerson* compares actual memory addresses being accessed by load and store instructions. Comparing the actual memory addresses in *Amerson* requires that the actual memory addresses be computed first. As a result, the detection of the load and store instructions in *Amerson* does not occur without “requiring computation of an external memory address” for the load and store instructions.

Regarding *Pickett*, the Office Action contains inconsistent statements regarding the teachings of *Pickett*. The Office Action first asserts that *Pickett* fails to show the “detection of instructions as [claimed]” in Claims 2 and 12. (*Office Action, Page 2, Section 3*). The Office Action then asserts that *Pickett* discloses a system that could detect instructions “without the need of calculating the memory address.” (*Office Action, Pages 6-7, Paragraph 16*). These positions regarding *Pickett* are completely inconsistent.

Moreover, the portions of *Pickett* cited in the Office Action (column 2, lines 2-34 and column 8, lines 64-65) contain absolutely no mention of detecting an “instruction that loads data from a first memory location that was previously stored to ... without requiring computation of an external memory address of said first memory location for the instruction” as recited in Claims 2 and 12. The first portion (column 2, lines 2-34) of *Pickett* simply recites how instructions with operands stored in memory may require multiple clock cycles to be executed, while instructions with operands stored in registers may require a single clock cycle to be executed. This portion of *Pickett* does recite that address calculation is not required for the operands stored in the registers. However, this portion of *Pickett* in no way recites detecting an

instruction, where the instruction is detected “without requiring computation of an external memory address of said first memory location for the instruction” as recited in Claims 2 and 12.

Similarly, the second portion (column 8, lines 64-65) of *Pickett* simply recites that an operand value is provided to a particular unit via a load/store unit 222 if the operand value is retrieved from a memory location. This portion of *Pickett* says absolutely nothing about detecting an instruction, where the instruction is detected “without requiring computation of an external memory address of said first memory location for the instruction” as recited in Claims 2 and 12.

For these reasons, the Office Action fails to show that the proposed *Pickett-Amerson* and *Amerson-Pickett* combinations disclose, teach, or suggest the Applicant’s invention as recited in Claims 2 and 12 (and their dependent claims).

**B. THE AMERSON-SRINIVASAN COMBINATION**

As noted above in Section III, *Amerson* compares the actual memory addresses being accessed by load and store instructions. As a result, the detection of the load and store instructions in *Amerson* cannot occur without “requiring computation of an external memory address” for the load and store instructions.

Regarding *Srinivasan*, the Office Action cites column 1, lines 59-67. This portion of *Srinivasan* simply recites the use of content-addressable memory (CAM). When a value of a data word matches a value of a search word, information associated with the data word may be stored in or retrieved from a CAM cell without computing the address of the information.

First, the technique described in *Srinivasan* relates to storing and retrieving information to and from memory. Nothing in the cited portion of *Srinivasan* relates to detecting an instruction. More specifically, nothing in the cited portion of *Srinivasan* relates to detecting an “instruction that loads data from a first memory location that was previously stored to” without “requiring computation of an external memory address of said first memory location for the instruction” as recited in Claims 2 and 12.

Second, the technique described in *Srinivasan* relates specifically to content-addressable memory. The Office Action fails to cite any portion of *Amerson* indicating that *Amerson* uses content-addressable memory or that *Amerson* could be modified to use content-addressable memory. The Office Action also fails to cite any portion of *Srinivasan* indicating that the technique described in *Srinivasan* could be used with non-content-addressable memory.

For these reasons, the Office Action fails to show that the proposed *Amerson-Srinivasan* combination discloses, teaches, or suggests the Applicant’s invention as recited in Claims 2 and 12 (and their dependent claims).

**C. THE ENGBRETSSEN-BALL COMBINATION**

The Office Action acknowledges that *Engbretsen* does not disclose determining a relationship between memory locations without computing the “effective addresses” of the memory locations as recited in Claim 20.

The Office Action cites various portions of *Ball* as disclosing these elements of Claim 20. The cited portions of *Ball* recite that a simulator may receive a “trace file” associated with an

executed benchmark program. The trace file may have “effective memory addresses” for memory access instructions in the benchmark program. The effective memory addresses are used to simulate execution of the memory access instructions without requiring the simulator to compute the effective memory addresses.

Claim 20 recites that a relationship between memory locations is determined “without requiring computation” of “effective addresses” for the memory locations. In contrast, *Ball* specifically recites calculating the “effective memory addresses” of “memory access instructions” for inclusion in the “trace file.” The simulator then uses the effective memory addresses during simulation. It is impossible for the simulator of *Ball* to use the effective memory addresses unless some component of *Ball* first computes the effective memory addresses. It is also irrelevant which component of *Ball* actually calculates the effective memory addresses. The only issue is whether *Ball* operates “without requiring computation” of “effective addresses” for memory locations. *Ball* clearly states that the effective addresses for memory locations are used by the simulator, meaning that some component of *Ball* had to compute those effective addresses.

Because of this, both *Engbreetsen* and *Ball* fail to disclose, teach, or suggest determining a relationship between a “first memory location” and a “second memory location” without “requiring computation of [an] effective address” for the first memory location and without “requiring computation of [an] effective address” for the second memory location as recited in Claim 20. As a result, the proposed *Engbreetsen-Ball* combination fails to disclose, teach, or suggest all elements of Claim 20 (and its dependent claims).

Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejections and full allowance of Claims 2-7 and 12-17.

V. **CONCLUSION**

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

**SUMMARY**


If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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